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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/29/2003

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09/14/2006

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EXAMINER

WEI, ZHENG

ART UNIT

PAPER NUMBER

2194

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/748,384	Applicant(s) SHPEISMAN ET AL.	
	Examiner Zheng Wei	Art Unit 2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/29/03 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/29/03, 02/10/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the application filed on 12/29/2003.

The priority date for this application is: 12/29/2003

Claims 1-30 are pending and have been examined.

Information Disclosure Statement

2. The information disclosure statement filed 12/29/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 19-22 are rejected under 35 U.S.C. 112, first paragraph, because the apparatus only has a single element "circuitry", which is not capable of doing things without cooperating with other computer elements and thus is interpreted as a single means/single step claim under MPEP 2164.08(a).

A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 27-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 27-30: The machine-readable medium, which the applicant defined in the specification, could be a carrier wave that is only a form of energy that is non-statutory (Page 3, paragraph [0014], "Accordingly, as used herein, a machine-readable medium may, but is not required to, comprise such a carrier wave.").

The definition of the machine-readable medium does not limit to physical articles or objects which constitute a manufacture within the meaning of 101 and which are functionally and structurally interconnected with the instructions in such a manner as to enable the instructions to act as a computer component and realize their functionality. In addition, the claims cover an embodiment of non-functional descriptive material and are additionally non-statutory for that reason. The claims recite "data representing sequences of instructions", the broadest reasonable interpretation of which would not necessarily be in executable form (e.g., a word processor document with the underlying theory or logic of the instructions) and therefore would cover non-functional embodiments.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-7, 19 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Wuytack (Wuytack et al. US 6421809 B1)

Claim 1: Wuytack discloses a method comprising:

- Scheduling a sequence of machine-executable instructions; (Col.4, lines 35-37, "Said method or system involves an iterative procedure, starting from an initial scheduling of said data access instructions.")
- Creating a data layout based on the scheduled sequence of machine-executable instructions. (Col.4, lines 37-38, "An initial value of the optimization or valuation criterion is determined")

Claim 2: Wuytack further discloses the method of claims 1, wherein the data layout is created in accordance with colored conflict graph, (Fig.1, from "Conflict Graph" to "HL Synthesis", clearly indicates that data layout is created in accordance with colored conflict graph by "Memory Allocation & Assignment"), the colored conflict graph being based on the scheduled sequence of machine-executable instructions. (Col.4, lines 40-41, "Note that a conflict graph is only defined for a given schedule.")

Claim 3: Wuytack also discloses the method of claim 2, wherein the colored conflict graph comprises:

- a plurality of nodes, each corresponding to a unique data element accessed by one or more of the machine-executable instruction, and each of the plurality of nodes being assigned a color, each color representing a hardware resource; (Fig.1, data elements A, B, C, D and corresponding nodes A, B, C, D in Conflict Graph; Fig.3, "Chromatic Number"; Col.16,

lines 13-25, "Note that a c-coloring of a graph G is a partitioning of G's nodes...")

- a number of edges, wherein each edge, if any, represents a potential hardware resource conflict. (Fig.1, Conflict Graph; Col.3, lines 32-34, "binary edges representing data access conflicts")

Claim 4: Wuytack further discloses that the method of claim 3, wherein the hardware resource comprises a data bank in cache memory. (ABSTRACT, "A formalized method and a design system are described for part of the design decisions, related to memory...", It is inherent that memory includes cache memory and further include data bank in the cache memory.)

Claim5: Wuytack also discloses that the method of claim 4, wherein the hardware resource conflict comprises a plurality of the one or more machine-executable instructions accessing the data bank in a same execution cycle. (Col.3, lines 13-15, "Access conflicts may be described a single or intra-cycle conflicts..."; Col.8, lines 40-43, "the conflicts are accessibility conflicts: there is a conflict when two groups of scalars are accessed simultaneously")

Claim 6: Wuytack further discloses that the method of claim 4, wherein each edge that connects a pair of nodes that are assigned a same color represents a hardware resource conflict. (Col.16, lines 13-25, "Such that every two adjacent nodes belong to a different partition class. In the case, when the members of partition X_i are colored with color I , adjacent nodes will receive different colors.")

Claim 7, 19 and 27: Wuytack discloses a method comprising:

- Creating a conflict graph having a plurality of nodes and a number of edges, each node representing a data element accessed by at least one machine-executable instruction, and each edge, if any, connecting a pair of the plurality of nodes, and representing a potential hardware resource conflict; (Col.3, lines 30-54, "In a second aspect of the invention said extended conflict graph is an undirected hyper-graph, comprising of nodes representing said basic groups; binary edges representing data access conflicts between the two basic groups connected by said hyper edge.", Col.10, lines 19-25, "All basic group conflicts are collected in a conflict graph where the nodes correspond to basic groups and there is an edge between two nodes whenever the corresponding basic groups are in conflict.")
- Coloring the conflict graph to generate a colored conflict graph by assigning a color to each of the plurality of nodes, each color representing a hardware resource (Col.16, lines 13-25, "Not that a c-coloring of a graph G is a partitioning of G's nodes in c partition classes ...", "Such that every two adjacent nodes belong to a different partition class. In this case, when the members of partition X_i are colored with cooler I, adjacent nodes will receives different colors."); and
- Creating a data layout by mapping each data element to a memory location, the memory location mapping to a corresponding hardware

resource. (Col.3, lines 27-29, "Finally, a selection of an optimized memory organization satisfying at least of the constraints depicted by said optimized extended conflict graph, is performed.")

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wuytack (Wuytack et al. US 6421809 B1)

Claim 23: Wuytack discloses a system comprising:

- A memory having a sequence of machine-executable instructions that access a plurality of data elements in one or more memory locations;
(Col.1, lines 23-26, "The operation of an essentially digital system can essentially be described as a set of data access operations or instructions on data structures or variables, being stored in said memories")
- Circuitry (Fig.2, "shows an architecture of a digital device. A memory part comprising of a hierarchical, layered memory organization is shown.
Further datapaths, controllers and address generators are shown")

But does not explicitly disclose the memory including L2 cache has a plurality of data banks, each of the one or more memory locations mapping to one of the

plurality of data banks. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to treat L2 cache as the special case of memory bank. One would have been motivated to apply the same optimization method for memory to solve cache conflict problems for further improving system efficiency.

11. Claims 8, 9, 10-14, 20-22, 24-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wuytack (Wuytack et al. US 6421809 B1) in view of Aizikowitz (Aizikowitz et al., US 5,774,730)

Claims 8, 20, 24 and 28: Wuytack discloses that the method as in claims 7, 19, 27 and 23 above, but does not explicitly disclose details about how to assign color to each nodes. However, Aizikowitz discloses: for a given node of each of the plurality of nodes, assigning a color from a corresponding color set, the corresponding color set comprising at least one color from a community color set having a plurality of colors, the at least one color not being in one or more other color sets, the one or more other color sets corresponding to one or more nodes adjacent to the given node. (Col.11, lines 11-65, "Each bit vector 810 represents the colors used by any neighbor as a zero and represents colors unused by neighbors as a one. Thus, the set of available colors for our hypothetical node A is all the colors in the bit vector 810 for node A that contain a one ..."). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Aizikowitz's color assigning method to assign color for

the nodes of conflict graph. One would have been motivated to use Aizikowitz's method in Wuytack's invention to assign color for each of nodes in the conflict graph and further clearly indicates the possible hardware resource conflicts.

Claims 9, 21, 25 and 29: Wuytack and Aizikowitz disclose a method as in claims 8, 20, 24 and 27 above, Aizikowitz further discloses that the assigning a color from the corresponding color set comprises:

- Designating the given node as a first node, the first node being an uncolored node and corresponding to a first corresponding color set; (Col.11, lines 31-33, "Thus, the set of available colors for our hypothetical node A is all the colors in the bit vector 810 for node A that contain a one.")
- If the first corresponding color set is not empty, assigning a first color from the first corresponding color set to the first node; (Col.11, lines 49-58, "Next we test to see if there is more than one color available for node A, If only one color is available, the color is selected for node A. If more than one color is available ... ")
- If there are one or more second nodes, the one or more second nodes being uncolored and adjacent to the first node, and corresponding to one or more second corresponding color sets, removing the first color from each of the one or more second corresponding color sets. (Col.11, lines 59-65, "If all of A's neighbors are not colored, we determine the colors of the neighbors of A's uncolored constrained neighbors (step 732).")

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Aizikowitz's detail method to assign color for the nodes of conflict graph. Therefore, one would have been motivated to use Aizikowitz's detail steps in Wuytack's invention to assign color and construct corresponding color sets for second nodes and further reduce possible hardware resource conflicts.

Claim 10: Wuytack and Aizikowitz disclose a method as in claim 9 above, Aizikowitz further discloses if the first corresponding color set is empty, selecting one of the plurality of colors from the community color set. (Col.11, lines 31-33, "Thus, the set of available colors for our hypothetical node A is all the colors in the bit vector 810 for node A that contain a one."; Fig.7, steps 710 and 712 clearly point out that if "Neighbor Colors" equals to zero, "Available Colors" is "All Colors" according to the formula.). It would have been obvious to one having ordinary skill in the art at the time the invention was made to select color from "All Colors" set. Therefore, one would have been motivated to select color from community color set, because in this case, the corresponding color set is empty.

Claim 11: Wuytack and Aizikowitz disclose a method as in claim 10 above, Aizikowitz also discloses the selected color of the plurality of colors is a least-weighted conflict color. (Col.3, lines 16-20, "Each occurrence of one of these colors is weighted according to some predetermined criteria."; "Choosing the color with the most desirable weighted count results in a greater likelihood of

coloring critical nodes.”). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the least weighted conflict color as the desired conflict color. One would have been motivated to use the least-weighted conflict color to represent the hardware resource conflict with the smallest impact on performance.

Claim 12: Wuytack and Aizikowitz disclose a method as in claim 9 above, Aizikowitz further discloses that the first color is a color that minimizes memory usage. (Col.14, lines 2-7, “The selection of how to compute and store the color bit mask will be dictated by various compiler parameters, such as anticipated compile, size of memory need for data structures, etc. The present invention encompasses all methods for computing and/or storing color bit mask 1000”). It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the color that can minimize memory usage. Therefore, one would have been motivated to select the color that minimizes memory usage to save hardware memory resource and improve performance.

Claim 13: Wuytack and Aizikowitz disclose a method as in claim 12 above, Wuytack further discloses that minimizes memory usage comprises a color corresponding to a data size that is not divisible by a block size. (Col.3-4, “Said pair-wise basic group conflict cost take into account the sizes of said basic groups, the total amount of data accesses to said basic groups, the bit width and word size of said basic groups.” Col.14-15, “In an embodiment of the invention

said possible memory sharing term comprises a term being a function of the word size of the basic group of said binary edge with the smallest word size when said basic groups of said binary edge having non-overlapping life time and zero otherwise)

Claims 14, 22, 26 and 30: Wuytack discloses the methods as in claims 7, 19, 23 and 27 above, but does not explicitly disclose assigning a priority to each of the plurality of nodes. However, Aizikowitz discloses assigning a priority to each of the plurality of nodes. (Col.3, lines 15-20, "Each occurrence of one of these colors is weighted according to some predetermined criteria, such as the importance or priority of the color at that particular node."). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Aizikowitz's method to assign a priority to each nodes in Wuytack's conflict graph. One would have been motivated to assign the priority to those nodes in order to reduce the chance to assign the same color to an adjacent node and further reduce hardware resource conflict.

Claim 15: Wuytack and Aizikowitz disclose a method as in claim 14 above, Wuytack also discloses that method for determining a weight for each of the one or more edges connected to the given node. (Fig.7, Col.5, BRIEF DESCRIPTION OF THE DRAWINGS, "There probabilities are then multiplied with the conflict costs in order to obtain a weighted conflict cost"), but does not disclose assigning priority and ranking. However, Aizikowitz further discloses that assigning a

priority to each of the plurality of nodes comprises, for a given node of each of the plurality of nodes:

- Determining a weight for each nodes; (Col.9, line 47-65)
- Assigning to each node a priority corresponding to the weight; (Col.11, line 59-65)
- Ranking the plurality of nodes. (Col.11-12)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Wuytack's method determining the weight of the edge (conflict cost) and use Aizikowitz's method to assign priority and ranking to each nodes. One would have been motivated to combine these two methods together to weight the edges connecting to each node and then assign priority and ranking to each node in order to reduce the chance to assign the same color to an adjacent node and further reduce hardware resource conflict.

Claim 16: Wuytack and Aizikowitz disclose a method as in claim 15 above, Wuytack further discloses that determining the weight to a given one of each of the one ore more edges connected to the node comprises determining the weight based on a performance penalty associated with a hardware resource conflict represented by the given edge. (Col.17, lines 24-38,"These basic group conflict probabilities are multiplied with their respective conflict costs and summed to get the weighted conflict cost, one part of the CDO cost function.")

Claim 17: Wuytack and Aizikowitz disclose a method as in claim 14 above, Aizikowitz further disclose assigning priority to each of the plurality of nodes.

(Col.11, lines 59-65, "We the rank the colors according to priority. We then select the color for A that is the highest rank and that is also an available color.").

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to assign priority using Aizikowitz's method.

One would have been motivated to use this method in Wuytack's conflict graph to reduce the chance that a high conflict node will be assigned the same color as an adjacent node.

Claim 18: Wuytack and Aizikowitz disclose a method as in claim 17 above, Wuytack also discloses that the hardware resource comprises a data bank in cache memory. (ABSTRACT, "A formalized method and a design system are described for part of the design decisions, related to memory...", It is inherent that memory includes cache memory and further include data bank in the cache memory.). And Wuytack further discloses that the hardware resource conflict comprises a plurality of the one or more machine-executable instructions accessing the data bank in a same execution cycle. (Col.3, lines 13-15, "Access conflicts may be described a single or intra-cycle conflicts..."; Col.8, lines 40-43, "the conflicts are accessibility conflicts: there is a conflict when two groups of scalars are accessed simultaneously")

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Briggs et al. (5,249,295) discloses a digital computer register allocation and code spilling using interference graph coloring.
- Calder et al. (5,963,972) discloses a memory architecture dependent program mapping.
- Wallace (5,933,644) discloses a method and apparatus for conflict-based block reordering.
- Panda et al. ("Memory Data Organization for Improved Cache Performance in Embedded Processor Applications", ACM Transactions on Design Automation of Electronic Systems, Vol2, No.4, October 1997, Pages 384-409)

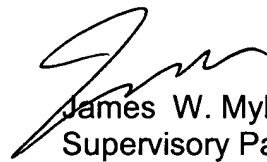
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zheng Wei whose telephone number is (571) 270-1059. The examiner can normally be reached on Monday-Thursday 14:00-15:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Myhre can be reached on (571) 270-01065. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2194

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ZW
09/05/2006



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09/05/2006